

ETS '07



European Test Symposium FINAL PROGRAM



Convention Center
Freiburg, Germany
20–24 May, 2007



tttc

Foreword

On behalf of the Steering and Program Committees, we would like to welcome you to the European Test Symposium 2007 (ETS'07), the largest event in Europe that is entirely devoted to presenting and discussing trends, emerging results, hot topics, and practical applications in the area of electronic-based circuit and system testing. ETS'07 is the 12th edition of this symposium, and it is held in Freiburg (Germany), the sunny capital of the Black Forest, in the heart of Europe close to the French and Swiss borders.

ETS continues its well-established format with one day of tutorials, a three-day technical program, and an attractive social event. The symposium's technical program consists of two plenary keynote addresses, technical paper presentations in three parallel sessions, four embedded tutorials, poster sessions, two panels, and one special session. Several test-related fringe events complete the "European Test Week", which includes the 3rd edition of the IEEE European Board Test Workshop and the 4th IEEE International Workshop on Silicon Debug and Diagnosis.

ETS'07 received a large number of contributions from all over the world, submitted to the scientific track, workshop track (including emerging ideas and case studies), vendor sessions, and special sessions. All submissions underwent a rigorous review process. For the scientific and workshop tracks, each paper has been reviewed on average by 6.8 reviewers. At a full-day TPC meeting, held on February 2, 2007 at Linköping, Sweden, all papers were discussed and evaluated. Based on the reviews and the discussions, 27 scientific track papers were selected for inclusion in the ETS'07 Formal Proceedings. In addition, 11 workshop track papers were selected, alongside 15 vendor session presentations; most of these have corresponding papers in the ETS'07 Informal Digest of Papers. Finally, 30 submissions were selected for poster presentations.

The European Test Symposium is the achievement of the contributions of many volunteers, who give generously their time to contribute to the success of the symposium. We would like to thank all for their efforts. We are confident that you will find EST'07 a productive and exciting experience, and would like to welcome you to Freiburg.

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Zebo Peng
Program Chair

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Program Vice-Chair

Christian Landrault
Publication Chair

Presentations are marked as follows:

-  formal
-  informal
-  vendor

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SUNDAY, MAY 20TH, 2007

The tutorials of ETS'07 are part of the annual IEEE Computer Society TTTC Test Technology Educational Program (TTEP) 2007.

<http://tab.computer.org/tttc/teg/ttep>



9:00–17:00 TTEP Tutorial 1

Practices in Analog, Mixed-Signal, and RF Testing

Salem ABDENNADHER : *Intel Corporation, USA* · Saghir A. SHAIKH : *Cadence Design Systems, USA*

Summary Most analog, mixed-signal and RF testing in industry today involves specification-based testing using Automatic Test Equipment (ATE). However, some companies employ alternative solutions to ATE testing that use DFT and BIST. This tutorial presents a brief overview of the industry practices in mixed-signal testing and RF testing. It includes testing examples of wired and wireless transceivers (an essential part of ultra high-speed networks). Plus, it discusses the testing challenges of System in Package (SiP), an emerging technology, and some of the feasible DFT solutions.

Intended Audience This tutorial is most suitable for design, test and DFT engineers involved in actual implementation of mixed-signal and wireless devices and systems. The architects and engineering managers would also greatly benefit from this tutorial.

Curriculum vitae Salem Abdennadher, Senior Staff DFX Engineer, Intel Corporation, has fourteen years of experience in mixed-signal design and DFT. Soon after graduating with Masters from Oregon State University 1992, he joined the industry and has worked with a research lab in France, Motorola, Level One Communications and Intel. His recent publications and international patent filing in mixed-signal DFT/BIST range from Filter BIST and On-chip Jitter BIST, to mixed-signal behavioral modeling and noise extraction and prediction.

Saghir A. Shaikh, Ph.D., Senior Core Competency Technical Leader at Cadence Design Systems, a graduate of the University of Texas at Austin 1996, Dr. Shaikh has eleven years of industrial experience in DFT at Intel Corporation, Sun Microsystems and Level One Communications, Inc. He has authored more than a dozen research papers which are presented in various conferences such as ITC, ICCAD, and VTS.

Both also have presented six tutorials through TTEP at ATS'04, LATW'05, VTS'05, ITC'05, ITC'06 and DATE'07 and are invited speakers for the ATS'05 industry challenges session.

Statistical Screening Methods targeting “Zero defect” IC Quality and Reliability Adit D. SINGH : *Auburn University, USA*

Summary The wide variation in normal process parameters now being observed in advanced semiconductor processes can sometimes cause the electrical impact of subtle manufacturing defects to remain within the acceptable range during test, thereby masking defect detection. Such undetected manufacturing flaws can potentially cause functional failure under untested operating conditions; they can also behave as latent reliability defects that “grow” over time to cause early life failure. Test methodologies that target “zero-defect” product quality requirements must address such test escapes by using innovative statistical methods to screen out passing parts that have a significant likelihood of field failure. Advanced screening methods fall into two broad categories: those that exploit the statistics of defect distribution on wafers – suspecting passing die in “bad” neighborhoods; and those that exploit the correlation in performance parameters on wafers – suspecting passing die that are performance outliers within local regions of the wafer. This tutorial will present screening methodologies that span both these categories, and illustrate their effectiveness using results from a number of recently published experimental studies on production circuits from IBM, Intel, LSI Logic, and NXP Semiconductor.

Intended Audience Test and Reliability Engineers, Engineering Managers, Reliability and Quality Assurance Managers, Researchers and Research Students.

Curriculum vitae Adit D. Singh is James B. Davis Professor of Electrical and Computer Engineering at Auburn University, where he directs the VLSI Design and Test Laboratory. His technical interests span all aspects of VLSI design, test and reliability. He has published about one hundred fifty research papers, served as a consultant to several major semiconductor companies, and holds international patents that have been licensed to industry.

Singh received the B.Tech from IIT Kanpur, and the M.S, and Ph.D. from Virginia Tech, all in Electrical Engineering. He is a Fellow of IEEE.

19:00 Welcome to Freiburg

Organ Concert Prof. Klemens Schnorr at the Marienorgel at the Freiburger Münster

The four organs of the Freiburger Münster were built in 1964/65. Main instrument is the Marienorgel on the left of transept (61 stops, 4 manuals and pedal), as well as the Choir organ built by Rieger, Schwarzach/Austria. The Choir organ was changed in 1990 and translated from the left to the right side. The organ in the main nave is built by Marcussen/Denmark, its organ case is inspired by the original instrument made by Jörg Ebert from Ravensburg in 1545. The 16th century sculptures of holy Mary (top) and the trumpet player (bottom) are still conserved. The organ on S. Michael choir in the tower was built by Freiburg organ builder Späth. All four organs with totally 136 stops can be played at the central console in the choir.



19:30–21:30 Welcome Reception

Historical Merchant House, Münsterplatz.
To find the location have a look at the map on page 17.



See your flash of inspiration go into production.

As a university graduate or intern, you'll be at the centre of the action in all phases of research, development and production. You'll work side by side with the experienced engineers whose resourcefulness and inventiveness have made our company so successful. With a staff of more than 4,000 and over 40 subsidiaries in Germany and abroad, we are one of the world's market and technology leaders in sensor electronics. We have ambitious plans for the future – and wide open doors for new talent. **Your ideas count.**

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MONDAY, MAY 21ST, 2007

8:30–9:00 Plenary Opening

Hans-Joachim Wunderlich : *Universität Stuttgart, DE*
ETS'07 Vice Program Chair

Welcome Address

Bernd Becker : *Universität Freiburg, Germany*
ETS'07 General Chair

Technical Program Introduction

Zebo Peng : *Linköpings Universitet, Sweden*
ETS'07 Program Chair

Presentation of ETS'06 Best Paper Award

Erik Jan Marinissen : *NXP Research, The Netherlands*
ETS'06 Program Chair

9:00–9:45 Keynote

If It's All About Yield, Why Talk About Testing?

Rene Segers : *NXP Semiconductors, The Netherlands*

Abstract This talk will discuss the evolution of test and diagnosis, in the broad sense, over the recent years as well as the outlook into the future. Test, as it was only recently a pure discriminator between good and bad, has gained significant more added value by acting also a feedback loop towards the manufacturing process of Integrated Circuits. Of course this feedback loop was already there, but was limited to information on test bin level from a tester. In the last couple of years, this has changed dramatically, and we are now able to pinpoint to circuit coordinates and/or to circuit structures as potential candidates for low yield causes. By linking this diagnosis information to in-line data, a more than direct link to a root cause in the fab can be achieved. And this is not the end of the story. By linking diagnosis to the layout one should be able to even stronger and quicker close the loop between Design, Manufacturing and Test. All of the above will be discussed in the talk, which in a sense could mean that the talk is all about DfX, Design for eXcellence...

Curriculum vitae After having finished his studies at the Technical University of Eindhoven, and after the then regular period of military service, Rene Segers started his career at Philips Research. There he led the introduction of DfT in general and digital scan-test in particular into Philips. Since those early days he had various positions in Philips, including Consumer Electronics, the Centre for Manufacturing Technology and Philips Semiconductors. Last year, together with more than 30.000 others, he joined NXP semiconductors where he is now DfX program manager. Until a couple of years ago Rene also acted as a professor in test technology at the Technical University in Eindhoven.

1 Invited Address

9:45–10:30

Electronics Design-For-Test: Past, Present and Future

Ben Bennetts : *Bennetts Associates, United Kingdom*

Abstract Do you know how many ENIAC vacuum tubes were replaced every day during its heyday? What did it teach us about Test, or Design-For-Test? Did Eldred really invent the stuck-at fault model in 1959? Is 99.999% fault cover all it's cracked up to be or are we fooling ourselves? Are we better off with 115% or even 80%? Where did Design-For-Test come from? Where is it now? Where's it heading? Is it true that boundary scan is the panacea of test? What are all these new Joint Test Action Groups – Internal, System and compact? Are they boondoggles, or are they serious?

Alongside all this, what does the price of oil, cheap airfares, global warming, text messaging for kids, sparrows in Leeuwarden, Skype, on-line social networking, IPTV, wearable electronics, Pat Gelsinger, Donald Rumsfeld, Clark Kent, Ella, Georgia and Emilie have to do with the future of test and DFT?

On the eve of his retirement after nearly 40 years in the test and DFT industry, the speaker will take a sometimes serious and sometimes irreverent look at the history, current status and projected future of the test and DFT industries, relating to various industries, various market segments (notably the hand-held consumer and telecommunication industries) and the way society is changing. Along the way many myths will be explored and dispelled, and social commentary added to explain certain projections.

Come, find out and be amused and amazed.

Curriculum vitae Dr R.G. "Ben" Bennetts was an independent consultant in Design-For-Test (DFT), consulting in product life-cycle DFT strategies, and delivering on-site and open educational courses in DFT technologies. During his career, he worked for LogicVision, Synopsys, GenRad and Cirrus Computers. Between 1986 and 1993, he was a free-lance consultant and lecturer on Design-for-Test (DFT) topics. During this time, he was a member of JTAG, the organization that created the original IEEE 1149.1-1990 Boundary-Scan Standard. He was a core-group member of IJTAG and SJTAG (and currently the SJTAG Chairman Emeritus), a co-founder and past Program Chair of the IEEE Board Test Workshop, a Steering Committee member of the IEEE European Test Workshop/Symposium for many years, founder of the IEEE European Board Test Workshop, and the founder and ex-Chairman of the IEEE's BTTAC organisation.

During the period 1968–2006, he published over 100 papers plus three books on test and DFT subjects. He retired from all DFT teaching and most DFT consulting on 31 December, 2006.

2A Fault and Defect Diagnosis

11:00–12:30

Janusz Rajski : *Mentor Graphics, USA*
 Laroussi Bouzaïda : *ST Microelectronics, FR*

Adaptive Debug and Diagnosis Without Fault Dictionaries

Stefan HOLST · Hans-Joachim WUNDERLICH : *Universität Stuttgart, Germany*

Interconnect Open Defect Diagnosis with Minimal Physical Information Chen LIU : *University of Iowa, USA* · Wei ZOU : *Mentor Graphics, USA* · Sudhakar M. REDDY : *University of Iowa, USA* · Wu-Tung CHENG · Manish SHARMA · Huaxing TANG : *Mentor Graphics, USA*

DERRIC: a Tool for Unified Logic Diagnosis

Alexandre ROUSSET · Alberto BOSIO · Patrick GIRARD · Christian LANDRAULT · Serge PRAVOSSOUDOVITCH · Arnaud VIRAZEL : *LIRMM, France*

11:00–12:30 Mixed Signal DFT and Test

2B

Andrew Richardson : *Lancaster University, UK*
S. Kajihara : *Kyushu Institute of Technology, JP*

A Digitally Testable Capacitance-Insensitive Mixed-Signal Filter

Erik SCHÜLER · Marcelo NEGREIROS : *Universidade Federal do Rio Grande do Sul, Brazil* · Pascal NOUET : *LIRMM, France* · Luigi CARRO : *Universidade Federal do Rio Grande do Sul, Brazil*

Reducing the Influence of DC Offset Drift in analog IPs using the Thue-Morse Sequence as Stimulus

Jan SCHAT : *NXP, Germany*

Using current testing to improve test coverage in mixed-signal IC testing

Yang ZHONG : *RWTH Aachen University, Germany* · Liqun FANG · Henk VAN DE DONK : *NXP Semiconductors, The Netherlands*

11:00–12:30 Advanced DFT Tools

2C

Peter Muhmenthaler : *Infineon Technologies, DE*
Einar J. Aas : *Norwegian University of Science & Technology, NO*

A Review of Power Strategies for DFT and ATPG

Richard ILLMAN · Brion KELLER · Sandeep BHATIA : *Cadence, USA*

ScanBurst – Scan Infrastructure and Environment for Highly Effective At-Speed Testing

Stephen PATERAS · Peter SHIELDS : *LogicVision, USA*

Realizing yield improvements with YieldAssist: High Volume Scan Diagnosis and Analysis

Brady BENWARE : *Mentor Graphics, USA*

3A NoC Testing

14:00–15:30

Gert Jervan : *Tallinn University of Technology, EE*
 Krishnendu Chakrabarty : *Duke University, US*

Test Configurations for Diagnosing Faulty Links in NoC Switches Jaan RAIK · Raimund UBAR · Vineeth GOVIND : *Tallinn University of Technology, Estonia*

Optimization of NoC Wrapper Design Under Bandwidth and Test Time Constraints Fawnizu Azmadi HUSSIN · Tomokazu YONEDA · Hideo FUJIWARA : *Nara Institute of Science and Technology, Japan*

How to Implement an Asynchronous Test Wrapper for Networks-on-Chip Nodes Xuan-Tu TRAN · Jean DURUPT · François BERTRAND : *CEA-LETI, France* · Vincent BEROULLE · Chantal ROBACH : *INPG-LCIS, France*

3B Advances in RF Test

14:00–15:30

Jochen Rivoir : *Verigy, DE* · Abhijit Chatterjee : *Georgia Tech, US*

FPGA Architecture for RF Transceiver System and Mixed-Signal Low Cost Tests Ivo KOREN · Frank DEMMERLE · Roland MAY · Martin KAIBEL · Sebastian SATTLER : *Infineon Technologies, Germany*

Digital Generation of Signals for Low Cost RF BIST Marcelo NEGREIROS · Luigi CARRO · Altamiro SUSIN : *Universidade Federal do Rio Grande do Sul, Brazil*

Variance Reduction for Supply Ramp Based Cheap RF Test Alternatives Shaji KRISHNAN · René JONKER · Leon VAN DE LOGT : *NXP Semiconductors, The Netherlands*

3C Exciting Test Equipment

14:00–15:30

Yervant Zorian : *Virage Logic, US* · Gunnar Carlsson : *Ericsson, SE*

The FLEX Architecture – High Efficiency Multisite Test Martin STADLER : *Teradyne, Germany*

Scalable System Platform for Cost Effective Mixed Signal Test Solutions Bruce MacDONALD : *LTX, USA*

Solutions for Testing Complex SoCs Martin FISCHER : *Verigy, Germany*

15:30–16:30 Posters & Coffee Break

4

Primary Input Vectors to Eliminate from Random Test Sequences for Synchronous Sequential Circuits

Irith POMERANZ : *Purdue University, USA* ·

Sudhakar M.REDDY : *University of Iowa, USA*

Reducing Test Data Volume for Deterministic BIST Via Test-Point Insertion

Yang ZHAO · Dong XIANG :

Tsinghua University, China · Krishnendu CHAKRABARTY :

Duke University, USA

A Self-Correction Method for Change of Clock Signal Width

Yukiya MIURA : *Tokyo Metropolitan University, Japan*

On Improving Channel Utilization in Testing NoC-Based Systems

Jia LI : *Chinese Academy of Sciences, China* ·

Qiang XU : *The Chinese University of Hong Kong, Hong Kong* ·

Yu HU · Xiao-wei LI : *Chinese Academy of Sciences, China*

Logic Errors in CMOS circuits due to Simultaneous Switching Noise

Florence AZAÏS · Laurent LARGUIER ·

Michel RENOVELL : *LIRMM, France*

Towards a test vector independent test response analyser for NoCs

Kim PETERSÉN : *HDC AB, Sweden* ·

Johnny ÖBERG : *KTH, Sweden*

Analysis of Random Testbench for Data-Dominated Hardware Descriptions

Iñigo UGARTE · Pablo

SANCHEZ : *Universidad de Cantabria, Spain*

Accessibility to Embedded A/MS Cores: An Oscillation-Based S-R DFT

Rahebeh NIARAKI ASLI : *Iran University*

of Science and Technology, Iran · Zainalabedin NAVABI :

Northeastern University, USA · Sattar MIRZAKUCHAKI : *Iran*

University of Science and Technology, Iran · Michel

RENOVELL : *LIRMM, France*

Implementation of security extension for IEEE Std 1149.1 and analysis of possible attack scenarios

Franc NOVAK ·

Anton BIASIZZO : *Jozef Stefan Institute, Slovenia*

Pattern Generation for Composite Leakage Current Maximization

Ashesh RASTOGI · Kunal GANESHPURE ·

Alodeep SANYAL · Sandip KUNDU : *University of Massa-*

chusetts, USA

5A Diagnosis and Debug

16:30–18:00

John P. Hayes : *University of Michigan, US* · Bruno Rouzeyre : *LIRMM, FR*

Parallel Scan-Like Testing and Fault Diagnosis Techniques for Digital Microfluidic Biochips Tao XU · Krishnendu CHAKRABARTY : *Duke University, USA*

Communication-centric SoC Debug using Transactions Bart VERMEULEN · Kees GOOSSENS : *NXP Semiconductors, The Netherlands* · Remco VAN STEEDEN : *University of Twente, The Netherlands* · Martijn BENNEBROEK : *Philips Research, The Netherlands*

Debug Architecture of the En-II System-on-Chip Bart VERMEULEN · Sjaak BAKKER : *NXP Semiconductors, The Netherlands*

5B Simulation and Verification

16:30–17:30

Franco Fummi : *University Verona, IT*
Jaana Raik : *Tallinn University of Technology, EE*

Electrical Simulation Model of the 2T-FLOTOX Core-Cell for Defect Injection and Faulty Behavior Prediction in eFlash Memories Olivier GINEZ : *LIRMM, France* · Jean-Michel DAGA : *ATMEL, France* · Patrick GIRARD · Christian LANDRAULT · Serge PRAVOSSOUDOVITCH · Arnaud VIRAZEL : *LIRMM, France*

Test Circuit for Functional Verification of Automatically Generated Cell Library M. GOMEZ · C. SILVA · S. BAVARESCO · C. ALEGRETTI · G. SARTORI · L. ROSA Jr. : *Universidade Federal do Rio Grande do Sul, Brazil* · A. REIS : *Nangate, USA* · Renato RIBAS : *Universidade Federal do Rio Grande do Sul, Brazil*

5C Intelligent Test Flows

16:30–18:00

Bernd Koenemann : *Visiting Professor, Universität Bremen, DE*
Jerzy Tyszer : *Poznan University of Technology, PL*

Multiple Benefit by Adaptive Testing Gil BALOG : *OptimalTest, Israel*

New RF Test Technologies for lower cost and flexibility Bill BURROWS : *Aeroflex Test Solutions, United Kingdom*

Enabling DUT-ATE Interaction Frank GROSSMANN : *SPEA, Germany*

18:00 – 19:30 Panel

6A

Ben Bennetts : *Bennetts Associates, UK*

Logic BIST and Test-Data Compression: Friends or Foes?

Organizers: Ben Bennetts : *Bennetts Associates, UK*

Erik Jan Marinissen : *NXP Research, NL*

Abstract Just a few years ago, Logic BIST was presented as the one and only solution to virtually all test challenges: growing ATE costs, growing test application times, difficult test access to deeply embedded cores, etc. However, suddenly, in 2001, before mainstream acceptance of Logic BIST, the first commercial Test Data Compression tool was launched. This, and similar TDC products, seemed to have quickly gained foothold in the DfT market. This panel will address the following questions: Did TDC tools actually erode the market for Logic BIST tools? How do TDC and Logic BIST compare, in benefits and costs? Is the success of TDC a temporary thing, while the long-term solution still has to come from Logic BIST? What are companies offering or using today, and how do they expect that to change in the medium- and long-term future? Is the DfT space per chip big enough for both approaches to co-exist?

Panelists

Davide Appello : *ST Microelectronics, Italy*

Friedrich Hapke : *NXP Semiconductors, Germany*

Richard Illman : *Cadence Design Systems, United Kingdom*

Steve Sunter : *LogicVision, Canada*

Jürgen Alt : *Infineon Technologies, Germany*

Janusz Rajski : *Mentor Graphics, USA*

Tom Williams : *Synopsys, USA*

18:00 – 19:00 Embedded Tutorial

6B

Patrick Girard : *LIRMM, FR*

Low Power Test

Nicola NICOLICI : *McMaster University, Canada* · Xiaoqing

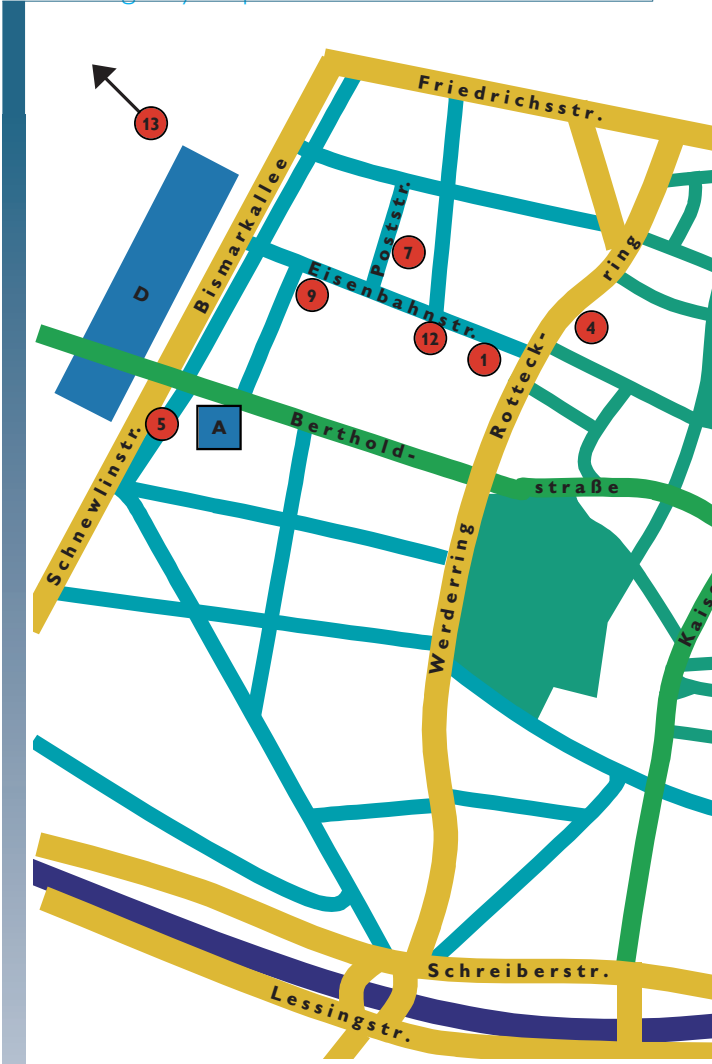
WEN : *Kyushu Institute of Technology, Japan*

Abstract Excessive power during test affects the reliability of digital integrated circuits, test throughput and manufacturing yield. Numerous low power test methods have been investigated over the past decade and new power-aware automatic test pattern generation, design-for-test and test planning techniques have emerged. This embeded tutorial introduces the topic of low power test and it overviews the basic techniques and some recent advancements in this field.

20:00 Dinner

Location to be announced

Freiburg City Map



- A ETS'07 site
Convention Center
- B Reception site
Historical Merchant House
- C Tutorial site
Katholische Akademie
- D Central train station

Sunday, May 20

09:00–10:30

TTEP Tutorials
Katholische Akademie

10:30–11:00

Coffee

11:00–12:30

TTEP Tutorials

12:30–13:30

Lunch

13:30–15:00

TTEP Tutorials

15:00–15:30

Coffee

15:30–17:00

TTEP Tutorials

17:00–18:30

Registration
Dorint Hotel

19:00–19:30

Organ Concerto
Münster

19:30–21:30

Welcome Reception
Historical Merchant House

Monday, May 21

08:00–08:30

Registration
Concert House

08:30–10:30

8:30 Plenary Opening
9:00 Keynote
9:45 Invited Address

1

10:30–11:00

Coffee

11:00–12:30

Fault and Defect Diagnosis A
Mixed Signal DFT and Test B
Advanced DFT Tools C

2

12:30–14:00

Lunch

14:00–15:30

NoC Testing A
Advances in RF Test B
Exciting Test Equipment C

3

15:30–16:30

Posters & Coffee

4

16:30–18:00

Diagnosis and Debug A
Simulation and Verification B
Intelligent Test Flows C

5

18:00–19:30

Panel A
Embedded Tutorial B

6

20:00

Dinner

Tuesday, May 22

08:30–10:00	7
Memory Test	A
Delay Faults, IEEE I500, SJTAG	B
Key Tech: Electrical Contacts	C

10:00–11:00	8
Posters & Coffee	

11:00–12:30	9
On-Line Testing and Self-Test	A
Fault Grading and Test Quality	B
Test Communities	C

12:30–14:00	
Lunch	
ETTC meeting	

14:00–15:00	10
Embedded Tutorials	

15:30–23:00	
Social Event	
<i>Staufen</i>	
<i>Badenweiler</i>	

Wednesday, May 23

08:30–10:00	11
Diagnosis & Yield Improvement	A
Single Event Upsets	B

10:00–11:00	12
Posters & Coffee	

11:00–12:30	13
Panel	A
Special Session	B

12:30–14:00	
Lunch	

14:00–15:30	14
Delay and Performance Test	

15:30–16:00	15
Closing Session	

16:00–19:00	
Workshops: EBTW & SDD	

Thursday, May 24

08:30–17:00	
Workshops continued	

TUESDAY, MAY 22ND, 2007

7A Memory Test

8:30-10:00

Matteo Sonza Reorda : *Politecnico di Torino, IT*
 Jean-Michel Daga : *Atmel, FR*

PPM Reduction on Embedded Memories in System on Chip Said HAMDIOUI · Zaid AL-ARS : *Delft University of Technology, The Netherlands* · Javier JIMENEZ · Jose CALERO : *Design of Systems on Silicon DS2, Spain*

An Integrated Built-in Test and Repair Approach for Memories with 2D Redundancy Philipp ÖHLER · Sybille HELLEBRAND : *Universität Paderborn, Germany* · Hans-Joachim WUNDERLICH : *Universität Stuttgart, Germany*

Dynamic Two-Cell Incorrect Read Fault due to Resistive-Open Defects in the Sense Amplifiers of SRAMs Alexandre NEY · Patrick GIRARD · Christian LANDRAULT · Serge PRAVOSSOUDOVITCH · Arnaud VIRAZEL : *LIRMM, France* · Magali BASTIAN : *Infineon, France*

7B Delay Faults, IEEE 1500 and IJTAG/SJTAG

8:30-10:00

Nicola Nicolici : *McMaster University, CAN*
 Elena Gramatova : *Slovak Academy of Sciences, SK*

Delay Fault Testing of Interconnect Logic Between Embedded Cores Ramesh TEKUMALLA : *Advanced Micro Devices, USA*

A Smart Delay Testing Framework based-on IEEE 1500 Po-Lin CHEN · Hao-Hsuan CHIU · Jhih-Wei LIN · Tsin-Yuan CHANG : *Tsinghua University, Taiwan*

Extended STAPL as SJTAG engine Johan HOLMQVIST : *Linköpings Universitet, Sweden* · Gunnar CARLSSON : *Ericsson, Sweden* · Erik LARSSON : *Linköpings Universitet, Sweden*

7C Key Technology: Electrical Contacts

8:30-10:00

Joan Figueras : *UPC, ES* · Carsten Wegener : *Infineon, DE*

Probing Challenges for Next Generation SoC Devices Sergio PEREZ : *FormFactor, USA*

New Low Inductance Socket Technology for High Speed Memory Device Testing

Joachim MOERBT : *Advantest, Germany*

Multi-site Test – Extraordinary DFT Desired

Peter MUHMENHALER : *Infineon Technologies, Germany*

10:00 – 11:00 Posters & Coffee Break

8

Defect-Tolerant N²-Transistor Structure for Reliable Design at the Nanoscale

Aiman EL-MALEH : *King Fahd University of Petroleum & Minerals, Saudi Arabia* · Bashir AL-HASHIMI : *University of Southampton, United Kingdom* · Ahmad AL-YAMANI : *King Fahd University of Petroleum & Minerals, Saudi Arabia*

Delay Testing for Application-Specific Interconnects of FPGAs based on Inphase Structure

Satoshi OHTAKE · Kosuke YABUKI · Hideo FUJIWARA : *Nara Institute of Science and Technology, Japan*

The Effects of Static Test Compaction for Functional Test Sequences on the Coverage of Stuck-at and Transition Faults

Irith POMERANZ : *Purdue University, USA* · Sudhakar M. REDDY : *University of Iowa, USA*

Learning from Failure Analysis: a case study

Federico BARONTI · Roberto RONCELLA · Roberto SALETTI : *University of Pisa, Italy* · Paolo D'ABRAMO · Luca DI PIRO · H. FABIAN · Monica GIARDI : *AustriaMicroSystems, Italy*

SAT-based ATPG for Path Delay Faults in Industrial Circuits

Stefan EGGERSGLÜSS · Görschwin FEY · Rolf DRECHSLER : *Universität Bremen, Germany* · Andreas GLOWATZ · Friedrich HAPKE · Juergen SCHLOEFFEL : *NXP Semiconductors, Germany*

A Novel Circuit-Oriented SAT Engine and Its Application to Unbounded Model Checking

Yang ZHAO · Tao LV · Lingyi LIU · Hua-wei LI · Xiao-wei LI : *Chinese Academy of Sciences, China*

A Pattern Selection Approach for Accelerating Soft Error Rate Testing

Alodeep SANYAL · Kunal GANESH PURE · Sandip KUNDU : *University of Massachusetts, USA*

Reliable Measurement of Interconnect Delays in Presence of Crosstalk-Induced Noise

Michal KOPEĆ : *University of Silesia in Cieszyn, Poland* ·
 Tomasz GARBOLINO · Krzysztof GUCWA · Andrzej
 HLAWICZKA : *Silesian University of Technology, Poland*

Soft-Error Tolerant Built-In Self-Test Scheme for Random Access Memories

Tsu-Wei TSENG · Chun-Hsien WU ·
 Jin-Fu LI : *National Central University, Taiwan*

ADL-driven Test Pattern Generation for Functional Verification of Embedded Processors

Anupam CHATTOPADHYAY : *ISS, Germany* · Arnab
 SINHA : *CSE, IIT Kharagpur, India* · Diandian ZHANG ·
 Rainer LEUPERS · Gerd ASCHEID · Heinrich MEYR : *ISS,
 RWTH Aachen University, Germany*

9A On-Line Testing and Self-Test 11:00–12:30

Luigi Carro : *UFRGS, BR* · Xiao-wei Li : *Chinese Academy of Science, CN*

A novel approach for online sensor testing based on an encoded test stimulus

Norbert DUMAS · Zhou XU ·
 Konstantinos GEORGOPOULOS : *Lancaster University,
 United Kingdom* · John BUNYAN : *QinetiQ, United Kingdom* ·
 Andrew RICHARDSON : *Lancaster University, United Kingdom*

Selecting Power-Optimal SBST Routines for On-Line Processor Testing

Andreas MERENTITIS · Nektarios
 KRANITIS · Antonis PASCHALIS : *University of Athens, Greece*
 · Dimitris GIZOPOULOS : *University of Piraeus, Greece*

Optimal Contexts for the Self-Test of Coarse Grain Dynamically Reconfigurable Processors

Tomoo INOUE · Takashi FUJII · Hideyuki ICHIHARA :
Hiroshima City University, Japan

9B Fault Grading and Test Quality 11:00–12:30

Joao Paulo Teixeira : *IST/INESC-ID, PT*
 Hideo Fujiwara : *Nara Institute of Science and Technology, JP*

A Seed-Selection Method to Increase Defect Coverage for LFSR-Re seeding-Based Test Compression

Zhanglei WANG · Krishnendu CHAKRABARTY : *Duke Uni-
 versity, USA* · Michael BIENEK : *Advanced Micro Devices, USA*

Ultra Fast Parallel Fault Analysis on Structurally Synthesized BDDs Raimund UBAR · Sergei DEVADZE · Jaan RAIK · Artur JUTMAN : *Tallinn University of Technology, Estonia*

Computation and Application of Absolute Dominators in Industrial Designs René KRENZ-BÅÅTH · Andreas GLOWATZ · Juergen SCHLOEFFEL : *NXP, Germany*

11:00–12:30 Test Communities

9C

Christian Landrault : *LIRMM, FR* · Erik Larsson : *Linköpings Universitet, SE*

Semiconductor Test Consortium Expands its Charter
Klaus LUTZ : *Advantest, Germany*

STC – Working Group Docking and Interface
Florian PUTZ : *esmo, Germany*

The STC's University Working Group Drives Alignment of Industry Paul RODDY : *Semiconductor Test Consortium STC, USA*

14:00–15:00 Embedded Tutorial

IOA

Bashir Al-Hashimi : *University of Southampton, UK*

System-in-Package, a combination of challenges and solutions Philippe CAUVET : *NXP, France* · Serge BERNARD · Michel RENOVELL : *LIRMM, France*

Abstract System-in-Package (SiP) has recently become a significant technology in the semiconductor industry, offering to the consumer applications many new product features without increasing the overall form factor. In this talk, the basic SiP concepts are first discussed, showing difference between SiP and SoC, illustrated by some examples, drawn from real-life cases. The specific challenges are considered from the testing point of view, focussing on the assembled yield and defect level for the packaged SiP. Various bare-die test techniques to find known-good-dies are described including their limitations, followed by two techniques to test the SiP at the system level: functional system test and embedded component test. A brief discussion on future SiP design and test challenges concludes the presentation.

IOB Embedded Tutorial

14:00–15:00

Paolo Prinetto : *Politecnico di Torino, IT***IC Test Cost Benchmarking**Klaus LUTHER : *Infineon Technologies, Germany*

Abstract Driven by the increasing complexity of integrated circuits the pressure on test cost reduction increases exponentially as productivity on chip level progresses according to Moore's Law. A high-level strategic approach for test cost target setting and planning will be explained. The intention is to keep cost of test constant relative to overall cost of goods sold. This method has been developed and used at Infineon over the last couple of years to align our location, equipment and productivity target setting.

IOC Embedded Tutorial

14:00–15:00

Hans Kerkhoff : *University of Twente, NL***Wafer Level Reliability Screens**Peter MAXWELL : *Micron Technology, USA*

Abstract This tutorial discusses test methods and voltage stress approaches required to ensure effective cost effective defect screening to produce high quality, reliable products. Wafer level reliability screens (WLRS) refers to the application of screens during wafer test that will both activate and detect a sufficient number of defects so that early life failure rate (ELFR) is reduced enough to meet customer spec, preferably without doing burn-in. Further, these screens have to have acceptable yield loss and acceptable test times

Social Event

15:30–23:00

A stop over in Staufen with Black Forest Cake

Staufen is one of the most picturesque villages in the south of Baden, situate amid magnificent vineyards. More than 1200 years of history, Staufen offers peace and undisturbed tranquillity.

One of the most famous citizens of Staufen was Johann Georg Faust, the legendary alchemist and magician that probably lived in Staufen about 500 years ago.

Today the visitor can read on the wall of the Lions Inn: "...and it is told that the most powerful of devils, Mephistopheles, the one he called brother-in-law when he was still alive, broke his neck, after the pact had expired after 24 years, thus handing over his poor soul to never ending perdition" (in: The 16th century Chronicles of Zimmer).



Social Event continued

A Banquet in Badenweiler at Hotel Römerbad

The History of Badenweiler began in Roman times. In 75AD vassals of the Roman Emperor Vespasian discovered the healing springs, built in the first baths and named the place Aquae Villae or “water town”. The very well preserved ruins of the Roman Baths are one of the most interesting sights of the region. Warm Mediterranean air flows through the Belfort Gap. The Black Forest in the north and east shields the resort from cold winds and temperature fluctuations. Thanks to its situation at a height of 450m, Badenweiler offers splendid views over the Markgräferland and the Rhine Plain as far as the French Vosges.



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WEDNESDAY, MAY 23RD, 2007

8:30–10:00 Diagnosis & Yield Improvement IIA

Sybille Hellebrand : *Universität Paderborn, DE*
Aiman El-Maleh : *King Fahd University of Petroleum & Minerals, Saudi Arabia*

Analyzing Volume Diagnosis Results with Statistical Learning for Yield Improvement Huaxing TANG · Manish SHARMA · Janusz RAJSKI · Martin KEIM · Brady BENWARE : *Mentor Graphics, USA*

Diagnostic Test Generation Based on Subsets of Faults Irith POMERANZ : *Purdue University, USA* · Sudhakar M. REDDY : *University of Iowa, USA*

Compound Defects Diagnosis with Non-Compressed Patterns Yu HUANG · Wu-Tung CHENG · Ruifeng GUO : *Mentor Graphics, USA*

8:30–10:00 Single Event Upsets IIB

Cecilia Metra : *University of Bologna, IT* · José Luis Huertas : *IMSE-CNM, ES*

Static and Dynamic Analysis of SEU effects in SRAM-based FPGAs Luca STERPONE · Massimo VIOLANTE : *Politecnico di Torino, Italy*

Multiple SEU Tolerance in LUTs of FPGAs Using Protected Schemes Hamid Reza ZARANDI · Seyed Ghassem MIREMADI : *Sharif University of Technology, Iran* · Costas ARGYRIDES · Dhiraj PRADHAN : *University of Bristol, United Kingdom*

System level approaches for mitigation of long duration transient faults in future technologies

Carlos LISBÔA : *Universidade Federal do Rio Grande do Sul, Brazil* · Marcelo ERIGSON : *Instituto de Informatica UFRGS, Brazil* · Luigi CARRO : *Universidade Federal do Rio Grande do Sul, Brazil*

10:00–11:00 Posters I2

Exploiting Arithmetic Built-In Self-Test Techniques for Path Delay Fault Testing Øystein GJERMUNDNES · Einar J. AAS : *Norwegian University of Science and Technology, NTNU, Norway*

Efficient Search Space Pruning for Multi Valued SAT based ATPG Maheshwar CHANDRASEKAR · Michael HSIAO : *Virginia Tech, USA*

A Defect-Tolerant Architecture for End of Roadmap CMOS Maryam ASHOUEI : *Georgia Tech, USA* · Adit SINGH : *Auburn University, USA* · Abhijit CHATTERJEE : *Georgia Tech, USA*

Minimal March Tests for Dynamic Faults in Random Access Memories Gurgen HARUTYUNYAN · Valery VARDANIAN : *Virage Logic, Armenia*

An Efficient Method to Tolerate Multiple Bit Upsets in SRAM Memory Costas A ARGYRIDES : *University of Bristol, United Kingdom* · Hamid R. ZARANDI : *Sharif University of Technology, Iran* · Dhiraj PRADHAN : *University of Bristol, United Kingdom*

A Reconfigurable Broadcast Scan Compression Scheme Using Relaxation Based Test Vector Decomposition Aiman EL-MALEH · Mustafa ALI · Ahmad AL-YAMANI : *King Fahd University of Petroleum & Minerals, Saudi Arabia*

TAM design and Test Data Compression for SoC Test Cost Reduction Julien DALMASSO · Marie-Lise FLOTTES · Bruno ROUZEYRE : *LIRMM, France*

Bayesian estimation for an imperfect test and repair model Simon WILSON : *Trinity College, Ireland* · Suresh GOYAL : *Lucent Technologies Bell Labs, USA*

Test-Data Compression Based on Variable-to-Variable Re-usable Huffman Coding Chrisovalantis KAVOUSIANOS : *University of Ioannina, Greece* · Emmanouil KALLIGEROS · Dimitris NIKOLOS : *University of Patras, Greece*

Transistor Level Timing Analysis Considering Multiple Inputs Simultaneous Switching Li ZHENTAO · Shuming CHEN : *National University of Defence Technology, China*

11:00–12:30 Panel

13A

Ilia Polian : *Universität Freiburg, DE*

Error Tolerance: Are Good-enough Chips Good Enough?

Organizer: Ilia Polian : *Universität Freiburg, Germany*

Abstract The advent of nanoscale technologies is leading to more and more errors, both hard and soft, showing up in the circuits. Known fault tolerance approaches can help in solving the problem, but often at an prohibitively high cost. Error tolerance is a novel paradigm stating that circuits containing defects, or good-enough (rather than perfect) chips, can operate in a way acceptable with respect to an application. First experiments demonstrated that a significant share of single-stuck-at faults in MPEG and JPEG devices lead to an acceptable performance. This panel will address the following questions: Is error tolerance a concept suited to achieve adequate yields in inherently unreliable nanoscale technologies? What are the implications of error tolerance on the design, test and verification flows? Is the market willing to accept good-enough chips? Is error tolerance applicable to hard or soft errors? What are the limitations?

Panelists (to include)

Rob Aitken : *ARM, USA*

Abhijit Chatterjee : *Georgia Tech, USA*

Sandip Gupta : *University of Southern California, USA*

John P. Hayes : *University of Michigan, USA*

Jens Leenstra : *IBM R&D, Germany*

11:00–12:30 Special Session

13B

Erik Jan Marinissen : *NXP Research, NL*

**Test Access for Chips, Boards and Multi-Board Systems:
What is Really Needed?**

Organizers: Robert Ruiz : *Synopsys, USA*

Erik Larsson : *Linköpings Universitet, Sweden*

Abstract What do you do when chips on a board behave unexpectedly? How do you know if the errors originate from functional design bugs or physical manufacturing defects? Do you have access to the internal silicon signals for observation and/or stimulation? Can you access the signals even when chips are mounted on boards and placed into systems? Do JTAG and SJTAG initiatives help with this issue, or is something else needed?

Speakers (to include)

Bill Eklow : *Cisco, USA*

Gunnar Carlsson : *Ericsson, Sweden*

Jeff Rearick : *AMD, USA*

Bart Vermeulen : *NXP, The Netherlands*

14 Delay and Performance Test 14:00–15:30

Michel Renovell : *LIRMM, FR*
 Adam Osseiran : *Edith Cowan University, AUS*

Automatic generation of instructions to robustly test delay defects in processors Sankar GURUMURTHY · Ramtilak VEMU · Jacob ABRAHAM : *University of Texas, USA* · Daniel G. SAAB : *Case Western Reserve University, USA*

On the Automatic Generation of Test Programs for Path-Delay Faults in Microprocessor Cores
 Paolo BERNARDI · Michelangelo GROSSO · Edgar SÁNCHEZ · Matteo SONZA REORDA : *Politecnico di Torino, Italy*

Purely Digital BIST for any PLL or DLL
 Stephen SUNTER · Aubin ROY : *LogicVision, Canada*

15 Closing Session 15:30–16:00

Closing Remarks and Introduction to ETS'08
 Matteo Sonza Reorda : *Politecnico di Torino, Italy*
 ETS'08 General Chair

Workshops 16:00–19:00

3rd IEEE European Workshop on Board Test
 held in Conjunction with the IEEE ETS 2007.

4th IEEE International Workshop on Silicon Debug and Diagnosis held in Conjunction with the IEEE ETS 2007.

To be continued on Thursday, May 24.

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