Sunday, May 20

08:00	**Tutorial Registration**
09:00	**Tutorials**
10:30	**Coffee**
11:00	**Tutorials**
12:30	**Lunch**
13:30	**Tutorials**
15:00	**Coffee**
15:30	**Tutorials**
17:00	**Symposium Registration**
18:30	
19:00	**Organ Concerto**
19:30	**Welcome Reception**

Monday, May 21

08:00	**Symposium Registration**		
08:30	**Opening Session** Keynote Invited Address		
10:30	**Coffee**		
11:00	**2A** Fault and Defect Diagnosis	**2B** Mixed Signal DFT and Test	**2C** Advanced DFT Tools
12:30	**Lunch**		
14:00	**3A** NoC Testing	**3B** Advances in RF Test	**3C** Exciting Test Equipment and Solutions
15:30	**Poster Session 4** **Coffee**		
16:30	**5A** Diagnosis and Debug	**5B** Simulation and Verification	**5C** Intelligent Test Flows
18:00	**Panel 6A** Logic BIST and Test-Data Compression: Friends or Foes?	**ET 6B** Low Power Test	
19:30			
20:00	**Dinner**		

Tuesday, May 22

08:00	**Symposium Registration**		
08:30	**7A** Memory Test	**7B** Delay Faults, IEEE 1500 and IJTAG/SJTAG	**7C** Key Technology: Electrical Contacts
10:00	**Poster Session 8** **Coffee**		
11:00	**9A** On-Line Testing and Self-Test	**9B** Fault Grading and Test Quality	**9C** Test Communities
12:30	**Lunch**		
14:00	**ET 10A** System-in-Package (SiP),	**ET 10B** IC Test Cost Benchmarking	**ET 10C** Wafer Level Reliability
15:00			
15:30	**Social Event**		

Wednesday, May 23

08:00	**Symposium Registration**	
08:30	**11A** Diagnosis and Yield Improvement	**11B** Single Event Upsets
10:00	**Poster Session 12** **Coffee**	
11:00	**Panel 13A** Error Tolerance: Are Good-enough Chips Good Enough?	**Special 13B** Test Access for Chips, Boards and Multi-Board Systems: What is Really Needed?
12:30	**Lunch**	
14:00	**14** Delay and Performance Test	
15:30	**Closing Session**	
16:00	**Affiliated Workshop** **- SDD**	

Presentation Session
Poster Session
Vendor Session
Panel Session
Embedded Tutorial
Special Session